UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,254	11/03/2003	Larry Lee Schumacher	5854-00100	3682

35617 7590 06/11/2008

DAFFER MCDANIEL LLP
P.O. BOX 684908
AUSTIN, TX 78768

EXAMINER	
TECKLU, ISAAC TUKU	
ART UNIT	PAPER NUMBER
2192	
MAIL DATE	DELIVERY MODE
06/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/700,254	SCHUMACHER ET AL.	
	Examiner	Art Unit	
	ISAAC T. TECKLU	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/08/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 have been reexamined.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Razdow et al. (US 6,330,008 B1) in view of Nikhil et al. (US 5,499,349).

As per claim 1 (Currently amended), Razdow discloses a system of managing data utilizing one or more processors and a single operating system, (e.g. FIG. 1, 122 and processor-1 104, processor-2, 104 … and related text) comprising:

a plurality of map components, each map component having one or more ports for accepting data and for producing data (e.g. FIG. 5, element 167 and related text) and each map component encapsulating a particular dataflow pattern (e.g. FIG. 3 and FIG. 37 and related text);

compiler tools for organizing and linking said map components using said ports into ~~a~~ an executable dataflow application (col. 2: 45-55 "… representation of parallelized graph … parallel operator instance and its associated partitioned dataflow or data link …" and e.g. FIG. 6 and related text); and

an executor for creating and managing data communication among map components in the dataflow application (col. 4: 1-15 "… data flow graph being executed …" e.g. FIG. 3 and related text) and executing the dataflow application on said one or more processors with data supplied to the system (col. 8: 45-55 "… parallel execution of a data flow graph …").

Razdow substantially disclosed the invention as recited above. However Razdow was silent about "with each map component as a separate thread of execution" as recited in the claim. Nevertheless, as evidenced by the teaching of Nikhil "executing the dataflow application on said one or more processors with each map component as a separate thread of execution" (col. 9:50-60 "… execute data flow graphs…" and col. 10:11-25 "… execute these data flow graphs independently and in parallel …"). Therefore, it is respectfully submitted that it would have been obvious to one of ordinary skill in the art at the time the invention was made to process plurality of threads independently by using pipelining structure as once suggested by Nikhil (see col. 3:20-25 and e.g. FIG. 2).

As per claim 2, Razdow discloses the system of claim 1, the compiler including tools for visually creating composite components comprising other map components (e.g. FIG. 3 and

related text) and tools for visually assembling map components into a dataflow application (col. 8: 15-25 "… visualization of execution of a parallel data flow graph …").

As per claim 3, Razdow discloses the system of claim 1, at least one map component having properties determining map component design behavior (e.g. FIG. 5, element 167 and related text).

As per claim 4, Razdow discloses the system of claim 1, at least one map component having properties that affect map component execution behavior (e.g. FIG. 3 and FIG. 37 and related text).

As per claim 5, Razdow discloses the system of claim 1, at least one of the map components comprising a composite component encapsulating a particular dataflow pattern using other map components as subcomponents (e.g. FIG. 3 and FIG. 37 and related text).

As per claim 6, Razdow discloses the system of claim 1, at least one of the map components comprising a scalar map component to process a specific data transformation (e.g. FIG. 6 and related text).

As per claim 7, Razdow discloses the system of claim 1, at least one of said ports linked to transfer specific types of data (e.g. FIG. 5, element 167 and related text).

As per claim 8, Razdow discloses the system of claim 1, at least one of said ports initially defined as a generic port for processing generic types of data, said generic port being later synthesized to transfer a specific sub-type of data (col. 8: 45-55 "… parallel execution of a data flow graph …").

As per claim 9, Razdow discloses the system of claim 1, at least one of said ports being composite, comprising a plurality of hierarchical ports (e.g. FIG. 6 and related text).

As per claim 10, Razdow discloses the system of claim 1, at least one of said ports supporting multi-valued null data tokens (e.g. FIG. 15 and related text).

As per claim 12, Razdow discloses the system of claim 1, at least one of said map components being composite comprising a number of hierarchical dataflow graphs (col. 2: 45-55 "… representation of parallelized graph … parallel operator instance and its associated partitioned dataflow or datalink …" and e.g. FIG. 6 and related text).

As per claim 13, Razdow discloses the system of claim 1, the compiler operating to remove design time links between map components to produce a flat dataflow graph containing a plurality of map processes for execution (col. 2: 45-55 "… representation of parallelized graph … parallel operator instance and its associated partitioned dataflow or data link …" and e.g. FIG. 6 and related text).

As per claim 14, Razdow discloses the system of claim 1, the executor operating to assign a thread to each map process for parallel execution (e.g. FIG. 1 and related text).

As per claim 16 (Currently amended), Razdow discloses a method of transforming data in parallel processing environment comprising a single operating system and one or more processors (e.g. FIG. 1, 122 and processor- 1 104, processor-2, 104 … and related text) wherein: map components are assembled visually into an integrated dataflow application by linking the map components and the integrated dataflow application is executed in parallel by recognizing the linked processes within the map components and allocating a thread to each process (col. 2: 45-55 "… representation of parallelized graph … parallel operator instance and its associated partitioned dataflow or data link …" and e.g. FIG. 6 and related text).

Razdow substantially disclosed the invention as recited above. However Razdow was silent about "each map process is executed on its allocated thread substantially in parallel, and said data resides in memory accessible to each map process" as recited in the claim. Nevertheless, as evidenced by the teaching of Nikhil "each map process is executed on its allocated thread substantially in parallel, and said data resides in memory accessible to each map process" (col. 5:60-67 and col. 6:1-10 "… executing a give thread... within this thread is a local instruction ..." and col. 7:55-67 "... thread... associated with... next instruction to be executed in the current thread ..." and col. 9:50-60 "… execute data flow graphs…" and e.g. FIG. 11). Therefore, it is respectfully submitted that it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an ability to initiate a new

thread that can execute concurrently with the current thread as once suggested by Nikhil (see col. 7:60-67).

As per claim 17, Razdow discloses the method of claim 16, wherein a plurality of map processes read data tokens from input ports and write data tokens to output ports (e.g. FIG. 3 and related text).

As per claim 18, Razdow discloses a method of managing data comprising: accessing a library of map components at least some of said map components constituting a specific data transformation and having input and output ports (e.g. FIG. 11 and related text); assembling a dataflow application using map components from said library linked together using said ports; and executing the assembled dataflow application with source data (col. 2: 45-55 "… representation of parallelized graph … parallel operator instance and its associated partitioned dataflow or datalink …" and e.g. FIG. 6 and related text).

Razdow substantially disclosed the invention as recited above. However Razdow was silent about "by assigning a thread to each map component where said threads execute in parallel on said source data without partitioning " as recited in the claim. Nevertheless, as evidenced by the teaching of Nikhil "by assigning a thread to each map component where said threads execute in parallel on said source data without partitioning " (col. 5:60-67 and col. 6:1-10 "… executing a give thread... within this thread is a local instruction ..." and col. 7:55-67 "... thread... associated with... next instruction to be executed in the current thread ..." and col. 9:50-

60 "… execute data flow graphs…" and e.g. FIG. 2). Therefore, it is respectfully submitted that it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an ability to initiate a new thread that can execute concurrently with the current thread as once suggested by Nikhil (see col. 7:60-67).

As per claim 19, Razdow discloses the method of claim 18, including imposing properties on the map components during assembly constraining the assemblage of the dataflow application (col. 8: 45-55 "… parallel execution of a data flow graph …").

As per claim 20, Razdow discloses the method of claim 18, the map components including polymorphic ports, which declare status as input and output ports during assemblage (e.g. FIG. 11 and FIG. 15 and related text).

As per claim 21 (new), Razdow discloses the system of claim 14, the executor operating on a single CPU in a hyper thread architecture (e.g. FIG. 2 and related text).

As per claim 22 (new), Razdow discloses the system of claim 14, the executor operating on a multiple processor core with at least some threads assigned to different processors (col. 8: 45-55 "… parallel execution of a data flow graph …").

As per claim 23 (new), Razdow discloses the system of claim 14, the executor operating on multiple processors in a distributed network configuration (col. 8: 45-55 "… parallel execution of a data flow graph …" and e.g. FIG. 1 and related text).

As per claim 24 (new), Razdow discloses the method of claim 16, communication between said processes executing in parallel being managed by an executor separate from the operating system (e.g. FIG. 1, 118 and related text).

As per claim 25 (new), Razdow discloses the method of claim 18, including:

determining if a port will block execution of thread (see at least col. 3:50-60 "… data flow blockages …"); and

avoiding a deadlock by allowing the data queue to grow at said determined port (e.g. FIG. 3, 132 A and related text).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Razdow et al (US 6,330,008 B1) in view of Nikhit et al. (US 5,499,349) further in view of Wack et al. (US 7,095,852).

As per claim 11 (Currently Amended), neither Razdow nor Nikhil explicitly disclose the system of claim 1, at least one of said map components being encoded as an encrypted ~~XML~~ extensible markup language (XML) document. However Wack discloses encryption schemes can be used to encrypt any type of data, encryption of XML data objects is of special interest, because XML's ability to capture the structure and semantics of data makes new applications available for cryptographic processes. Therefore it would have been obvious to one skilled in the art at the time of the invention was made to encrypt the map component to capture structure and semantics of data to create new dataflow graph as once suggested by Wack (col. 7:45-55).

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Razdow et al (US 6,330,008 B1) in view Nikhit et al. (US 5,499,349) further in view of Yamanaka (US 6,993,753 B2).

As per claim 15, neither Razdow nor Nikhit explicitly disclose the system of claim 1, the compiler tools operating to perform syntactic and semantic analysis, type inference and validation. However, Yamanaka discloses a compiler of Fig. 1, which performs syntactic and semantic analysis of a source program. Therefore it would have been obvious to one skilled in the art at the time the invention was made to perform semantic and syntactic analysis to process

the verification process faster than in conventional method and to verify the hierarchical structure (map) as once suggested by Yamanaka (col. 1:45-55).

Response to Arguments

7. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection. See Nikhit et al. art made of record.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ISAAC T. TECKLU whose telephone number is (571)272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Isaac T Tecklu/
Examiner, Art Unit 2192

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192